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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/342,348	06/29/1999	TIMOTHY J. BROSNIHAN	07043/060002	6423

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EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/342,348	BROSNIHAN ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-12,23 and 25-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 7-12, 23 and 25-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on July 16, 2004 has been entered.

Status of the Claims

2. Amendment filed July 16, 2004 has been entered. Claims 28-31 have been added. Claims 6 and 24 have been canceled. Claims 1, 2, 7-10 and 25 have been amended. Claims 1-5, 7-12, 23 and 25-31 are pending.

Claim Objections

3. Claims 2, 29 and 30 are objected to because of the following informalities:

Claims 2, 29 and 30, line 2, recite: "the substrate".

The correct term should be: -- the device layer --.

Appropriate correction is required.

4. Claims 26 and 27 are objected to because of the following informalities:

Claims 26 and 27 are not part of the originally filed application, therefore, the status of claims 26 and 27 should be -- (Previously Presented) --.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5, 7-12, 23, 25 and 28-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bashir et al. (U.S. Patent No. 5,747,353) in view of Hunter et al. (U.S. Patent No. 4,631,803) all of record.

With respect to claim 1, Bashir teaches a method of fabricating a microelectromechanical system substantially as claimed including:

providing a substrate having a device layer (106), a handle layer (102) and a sacrificial layer (104) between the device layer (106) and the handle layer (102);

etching a first trench (121) in the device layer (106), the first trench surrounding a first region of the substrate;

forming an isolation layer (thermal oxidation) in the first trench (121) to form an isolation trench;

etching a second trench (120) in the device layer (106), the second trench (120) defining a microstructure (142/144) including a plurality of elements (144) laterally anchored to the

isolation trench such that the isolation trench (121) provides electrical isolation for the anchored elements (144) of the microstructure from each other; and

removing a portion of the sacrificial layer (104), wherein the removed portion entirely undercut the plurality of laterally anchored elements (144). (See Figs. 1-9, col. 3-col. 10).

Note that, the dielectric isolation layer of Bashir is formed by thermal oxidizing the exposed device layer (106) followed by depositing a polysilicon layer (similar to that of the present invention, page 12, line 27).

Thus, Bashir is shown to teach all the features of the claim with the exception of forming the isolation trench including depositing a dielectric isolation layer in the first trench.

However, Hunter teaches forming an isolation trench including: depositing a dielectric isolation layer (40) in the trench (36) to from an isolation trench. (See Fig. 2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the isolation trench of Bashir by depositing a dielectric isolation layer (40) in the first trench as taught by Hunter to eliminate the formation of defects in the surrounding semiconductor substrate.

With respect to claim 4, the method of Bashir further includes depositing a filler material (poly) over the isolation layer (thermal oxide) in the trench (121).

With respect to claim 5, in view of Hunter, the isolation layer fills the first trench.

With respect to claim 7, removing a portion of the sacrificial layer (104) of Bashir includes releasing the microstructure (See Fig. 8).

With respect to claims 8 and 9, etching the first (121) and second (120) trenches of Bashir etch through the device layer (106) to expose the sacrificial layer (104).

With respect to claim 10, the sacrificial layer (104) of Bashir includes silicon dioxide.

With respect to claim 11, wherein the device layer (106) of Bashir includes epitaxial silicon.

With respect to claim 12, the isolation layer (40) of Hunter includes silicon nitride.

With respect to claim 23, etching the second trench (120) of Bashir includes etching a portion of the device layer (106) that abuts the first trench (121). (See Fig. 8).

With respect to claim 25, etching the second trench (120) of Bashir includes forming at least one movable element (142) and at least one generally immobile element (144).

With respect to claim 28, removed a portion of the sacrificial layer (104) of Bashir at least partially undercuts the isolation trench (121). (See Fig. 8).

With respect to claim 29, the first trench (121) of Bashir surrounds a region of the device layer (106).

With respect to claim 30, the first trench (121) of Bashir electrically isolates a first region of the device from a second region of the device layer.

With respect to claim 31, the second trench (120) is located in the first region.

With respect to claim 2, the method of Bashir further includes forming circuitry in a second region of the device layer outside the first region.

With respect to claim 3, Bashir teaches deposition of a metal layer, patterning of the metal layer to define the contacts. (See col. 5, ll. 39-50).

Thus, Bashir is shown to teach all the features of the claim with the exception of explicitly disclosing the connection of the microstructure to the circuitry.

However, Bashir clearly implies the formation of the metal layer is to connecting the microcircuit to the control circuit in the second region.

6. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bashir '353 and Hunter '803 as applied to claim 1 above, and further in view of Peeters et al. (U.S. Patent No. 5,637,189) of record.

Bashir teaches the first and second trenches are etched using an anisotropic RIE etch process.

Thus, Bashir is shown to teach all the features of the claim with the exception of explicitly using ICP.

However, Peeters teaches inductively coupled plasma (ICP) is one of many etching process known in the art to be reactive ions etch (RIE). (See col. 7, lines 3-20).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to etch the first and second trench of Bashir using ICP etcher as taught by Peeters because this dry etch process is well suited for construction of dimensionally accurate microdevices.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 9:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Anh D. Mai
September 13, 2004